What is Claimed is:

1. An apparatus, comprising:

an electrically insulating body having at least two major surfaces;

a first plurality of electrical contacts disposed on a first major surface of the body, each having a thickness less than a first thickness, and an area less than a first area;

a second plurality of electrical contacts disposed on a second major surface of the body, each having a thickness greater than a second thickness, and an area greater than a second area;

a plurality of electrical vias disposed in the body, between the first major surface and the second major surface so as to provide electrically conductive paths between at least a portion of the first plurality electrical contacts and a corresponding portion of the second plurality of electrical contacts; and

an evacuation pathway and valve adapted for connection to a vacuum source;

wherein the first plurality of electrical contacts is disposed on the first major surface in a first two dimensional array with a repeating non-uniform pitch pattern, and the second plurality of electrical contacts is disposed on the second major surface in a second two dimensional array in a repeating uniform pitch pattern.

2. The apparatus of Claim 1, wherein the second area is greater than the first area.

3. The apparatus of Claim 2, wherein at least a portion of the first plurality of electrical contacts are adapted to make electrical contact with a corresponding plurality of contact pads of a plurality of non-singulated integrated circuits.

4. The apparatus of Claim 2, wherein the second plurality of electrical contacts comprise nickel plated copper.

5. The apparatus of Claim 2, wherein the second plurality of electrical contacts comprise gold.

6. An apparatus adapted for electrical testing, comprising:

a substrate including a plurality of non-singulated integrated circuits, the plurality of integrated circuits each having at least one terminal disposed on at least a first major surface of the substrate, the terminals adapted for electrical connection to an external device; and

a full wafer contacter attached to the first major surface of the substrate;

wherein the full wafer contacter comprises:

an electrically insulating body having at least two major surfaces;

a first plurality of electrical contacts disposed on a first major surface of the body;

a second plurality of electrical contacts disposed on a second major surface of the body;

a plurality of electrical vias disposed in the body, between the first major surface and the second major surface so as to provide electrically conductive paths between at least a portion of the first plurality electrical contacts and a corresponding portion of the second plurality of electrical contacts; and

an evacuation pathway disposed in the electrically insulating body, the evacuation pathway adapted to provide access to one or more gases; and

an evacuation pathway sealing means adapted to maintain a pressure established between the full wafer contacter and the substrate.

7. The apparatus of Claim 6, wherein the substrate comprises a wafer.

8. The apparatus of Claim 7, wherein the wafer is approximately circular with a first radius, the full wafer contacter is approximately circular with a second radius, and the second radius is less than the first radius.

9. The apparatus of Claim 8, wherein a pressure differential urges the full wafer contacter into electrical contact with the terminals.

10. The apparatus of Claim 8, wherein the full wafer contacter is removably attached to the wafer.

11. The apparatus of Claim 8, wherein the full wafer contacter is permanently attached to the wafer.

12. A method of electrically accessing a plurality of integrated circuits, each integrated circuit having a plurality of terminals, the method comprising:

providing a wafer having a first and a second major surface, the plurality of integrated circuits disposed on a first major surface thereof, each of the plurality of integrated circuits having a plurality of terminals, and the plurality of integrated circuits disposed over at least a portion of the first major surface;

providing a full wafer contacter having a first major surface and a second major surface, a first plurality of contact terminals disposed on the first major surface of the full wafer contacter in a pattern that corresponds to the terminal layout of the plurality of integrated circuits; and

removably attaching the full wafer contacter to the wafer such that the first major surface of the wafer and the first major surface of the full wafer contacter are facing each other, and such that at least a portion of the terminals of the integrated circuits are in electrical contact with the first plurality of contact terminals;

wherein each of the first plurality of contact terminals is electrically coupled to a corresponding one of a second plurality of contact terminals disposed on the second major surface of the full wafer contacter.

13. The method of Claim 12, wherein removably attaching comprises vacuum attaching.

14. The method of Claim 12, wherein removably attaching comprises producing a low pressure zone between the full wafer contacter and the wafer.

15. The method of Claim 14, wherein removably attaching comprises, in an atmosphere containing one or more gases, placing the full wafer contacter over the wafer, and evacuating at least a portion of the one or more gases disposed between the full wafer contacter and the wafer.

16. The method of Claim 12, wherein the integrated circuit terminals comprise bonding pads.

17. The method of Claim 12, wherein the integrated circuit terminals comprise solder bumps.

18. The method of Claim 12, further comprising aligning the full wafer contacter to the wafer such that the terminals of the integrated circuits and the terminals disposed on the first major surface of the full wafer contacter will be in electrical contact when the full wafer contacter is removably attached to the wafer.

19. The method of Claim 12, wherein a first portion of the plurality of integrated circuits has a first terminal layout pattern, and a second portion of the plurality of integrated circuits has a second terminal layout pattern, and the first and second terminal layout patterns are different.

20. The method of Claim 19, wherein each of the first portion of the plurality of integrated circuits has a first die size, and each of the second portion of the plurality of integrated circuits has a second die size, and the first and second die sizes are different.